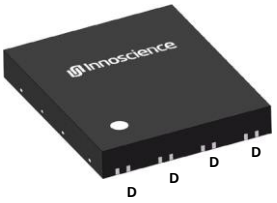
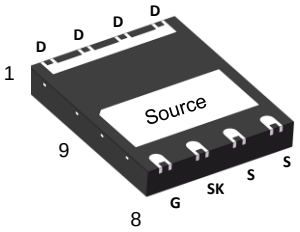
INN700DA480B

1. General description

700V GaN-on-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead package (DFN) with 5 mm × 6 mm size

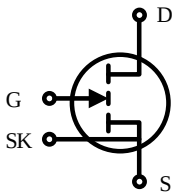
2. Features





- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

3. Applications



- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion

4. Key performance parameters

Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	700	V
$R_{DS(on),max}$ @ V_{GS} = 6 V	480	mΩ
$Q_{G,typ}$ @ V_{DS} = 400 V	1.3	nC
$I_{D,pulse}$	9	A
Q_{OSS} @ V_{DS} = 400 V	10.5	nC
Q_{rr} @ V_{DS} = 400 V	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
8	1, 2, 3, 4	7	5, 6, 9

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN700DA480B	DFN 5X6	70DA480B

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6. Maximum ratings

at T_j = 25 °C unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS, max}$	700	V	V_{GS} = 0 V, Tj = -55 °C to 150 °C
Drain source voltage transient [1]	$V_{DS, transient}$	800	V	V_{GS} = 0 V
Drain source voltage, pulsed [2]	$V_{DS, pulse}$	750	V	T_j = 25 °C; total time < 10 h
				T_j = 125 °C; total time < 1 h
Continuous current, drain source	I_D	5	A	T_c = 25 °C
Pulsed current, drain source [3]	$I_{D, pulse}$	9	A	T_c = 25 °C; V_{GS} = 6 V; t_{PULSE} = 10 µs
Pulsed current, drain source [3]	$I_{D, pulse}$	5	A	T_c = 125 °C; V_{GS} = 6 V; t_{PULSE} = 10 µs
Gate source voltage, continuous [4]	V_{GS}	-1.4 to +7	V	Tj = -55 °C to 150 °C
Gate source voltage, pulsed	$V_{GS, pulse}$	-20 to +10	V	Tj = -55 °C to 150 °C; t_{PULSE} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	40	W	T_c = 25 °C
Operating temperature	T_j	-55 to +150	˚C	
Storage temperature	T_{stg}	-55 to +150	˚C	

1. $V_{DS, transient}$ is intended for non-repetitive events, t_{PULSE} < 200 µs.
2. $V_{DS, pulse}$ is intended for repetitive pulse, t_{PULSE} < 100 ns.
3. Limit was extracted from characterization test, not measured during production.
4. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10.

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-ambient	R_{thJA} [1]	72	°C/W	
Thermal resistance, junction-case	R_{thJC}	3.05	°C/W	
Thermal resistance, junction-ambient	T_{sold}	260	°C	MSL3

1.R_{thJA} is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.

8. Electric characteristics

at T_j = 25 °C, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	I_D = 5.2 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.9	-		I_D = 5.2 mA; V_{DS} = V_{GS}; T_j = 150 °C
Drain-source leakage current	I_{DSS}	-	0.2	10	μA	V_{DS} = 700 V; V_{GS} = 0 V; T_j = 25 °C
		-	2	-		V_{DS} = 700 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	20	-	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	365	480	mΩ	V_{GS} = 6 V; I_D = 2 A; T_j = 25 °C
		-	790	-	mΩ	V_{GS} = 6 V; I_D = 2 A; T_j = 150 °C
Gate resistance	R_G	-	14	-	Ω	f = 5 MHz; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	43	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	13	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer capacitance	C_{rss}	-	0.1	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	18	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	26	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	10.5	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	2	-	ns	V_{DS} = 400 V; I_D = 4 A; L = 318 μH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 2 Ω; See Figure 22
Turn-off delay time	$t_{d(off)}$	-	3	-	ns	
Rise time	t_r	-	5	-	ns	
Fall time	t_f	-	7	-	ns	

1. $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.

2. $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	1.3	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 2 A
Gate-source charge	Q_{GS}	-	0.1	-	nC	
Gate-drain charge	Q_{GD}	-	0.5	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.7	-	V	V_{DS} = 400 V; I_D = 2 A

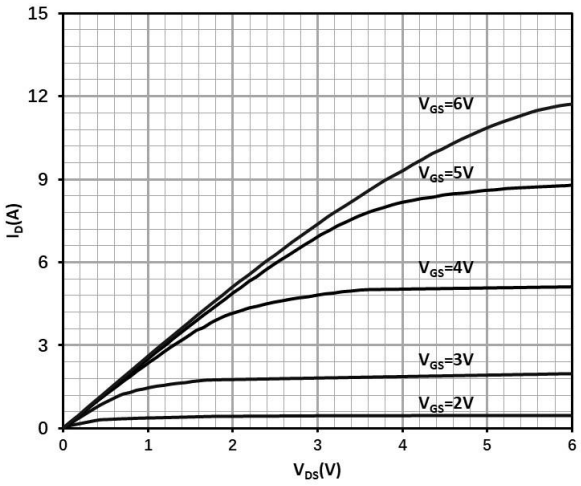
Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.8	-	V	V_{GS} = 0 V; I_S = 2 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	-	9	A	V_{GS} = 6 V; t_{PULSE} = 10 µs
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_S =2 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

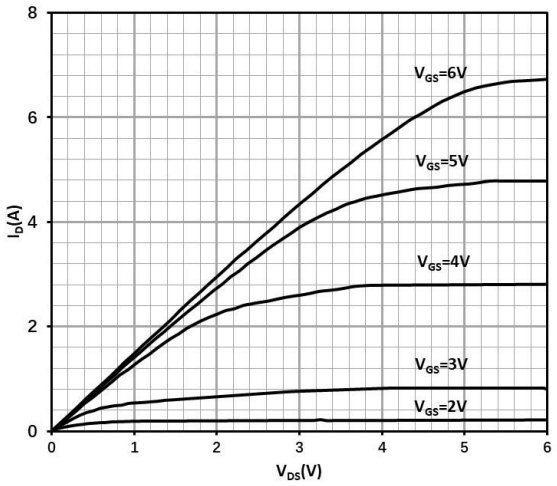
at T_j = 25 °C, unless specified otherwise

Figure 1 Typ. output characteristics



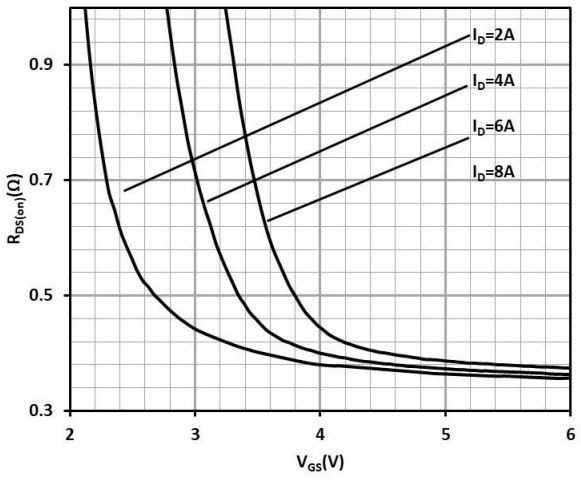
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



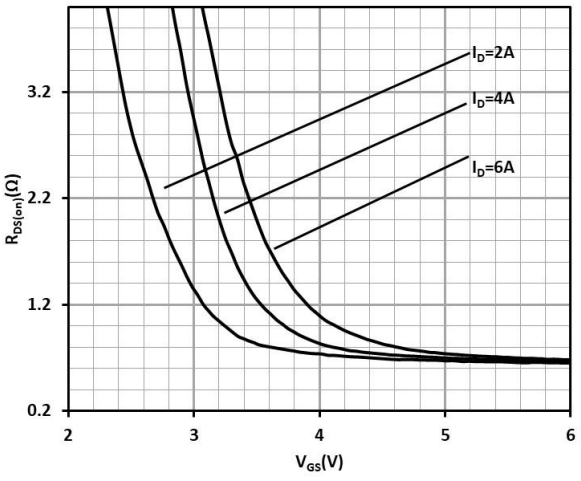
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 3 Typ. Drain-source on-state resistance



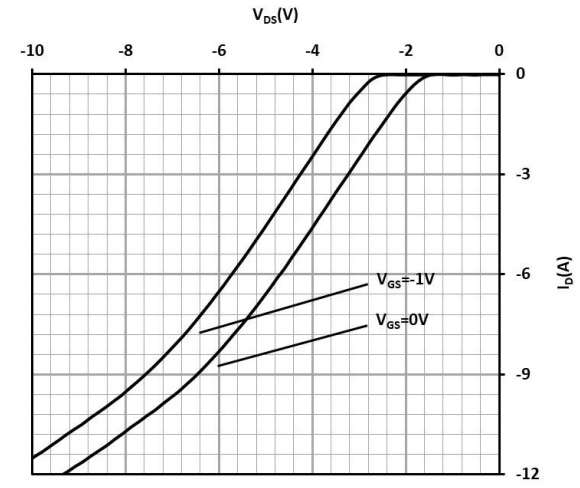
$R_{DS(on)} = f(I_D,V_{GS})$; T_j = 25 °C

Figure 4 Typ. Drain-source on-state resistance



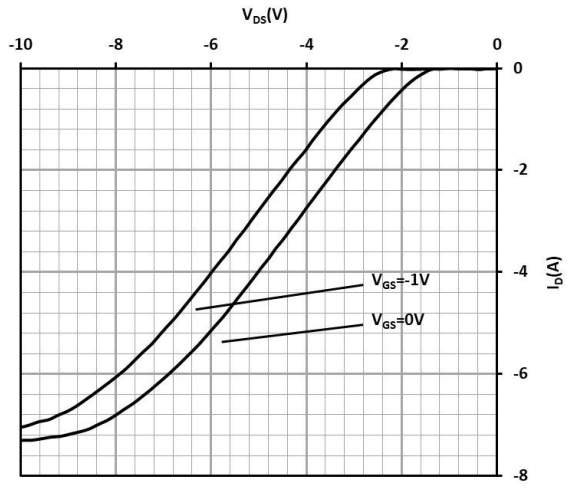
$R_{DS(on)} = f(I_D,V_{GS})$; T_j = 125 °C

Figure 5 Typ. channel reverse characteristics



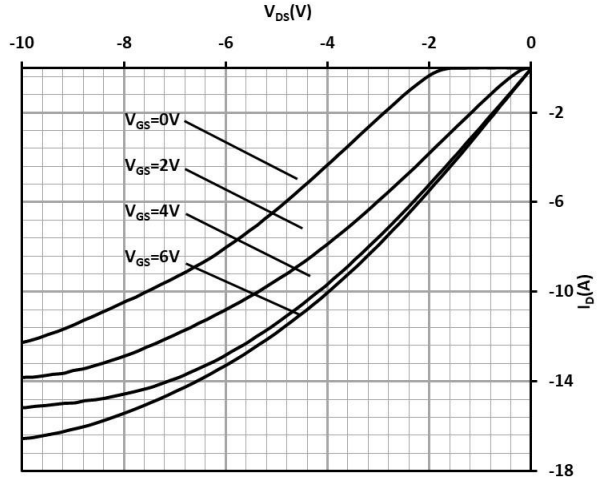
$I_D = f(V_{DS},V_{GS})$; T_j= 25 °C

Figure 6 Typ. channel reverse characteristics



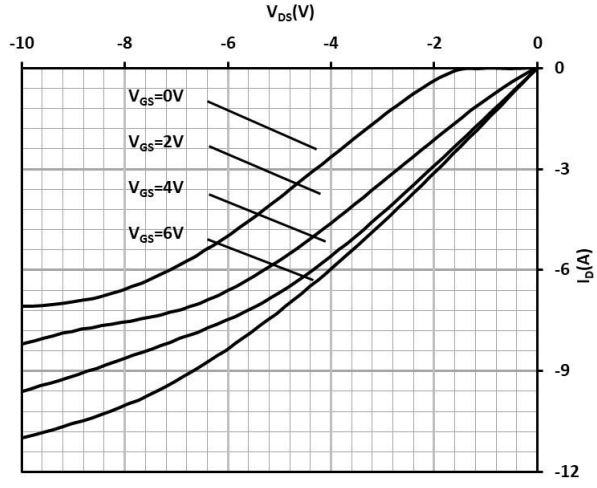
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 7 Typ. channel reverse characteristics



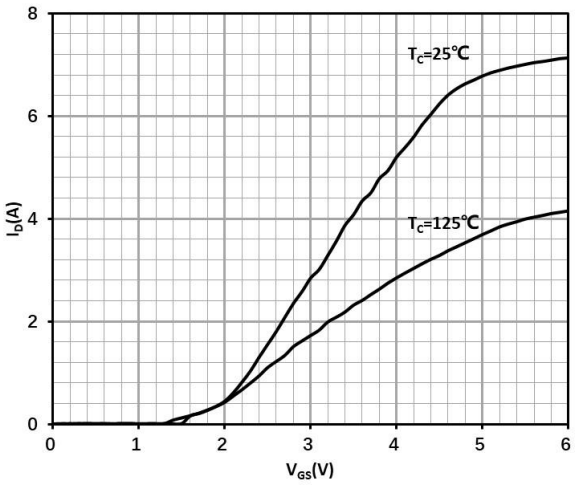
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C

Figure 8 Typ. channel reverse characteristics



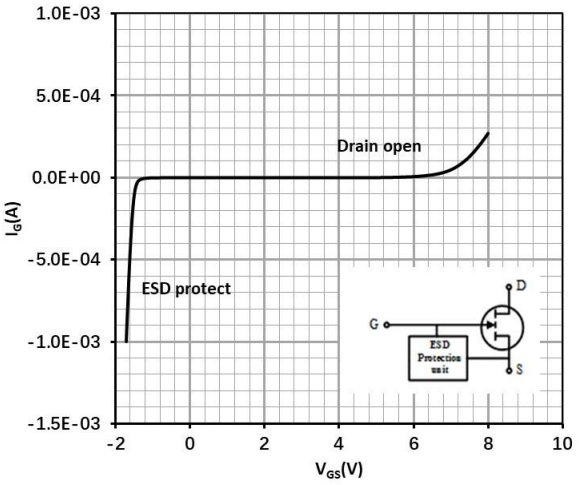
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 9 Typ. transfer characteristics



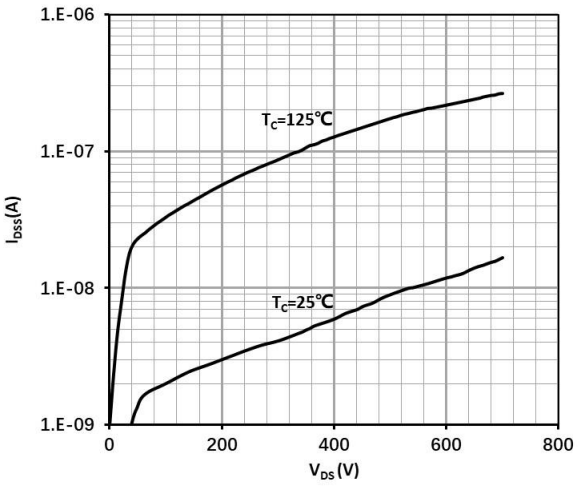
$I_D = f(V_{GS})$; V_{DS}= 3 V

Figure 10 Typ. Gate-to-Source leakage



$I_G = f(V_{GS})$; I_G reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



$I_{DSS} = f(V_{DS})$; V_{GS} = 0 V

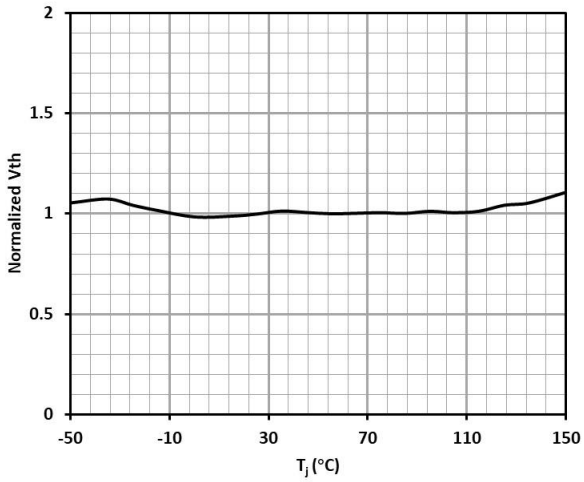
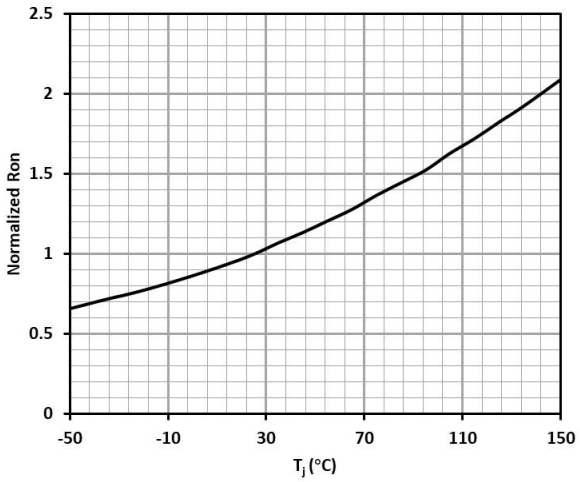
Figure 12 Gate threshold voltage	Figure 13 Drain-source on-state resistance
	
V_{TH} = f(T_j); V_{GS} = V_{DS}; I_D = 5.2 mA	$R_{DS(on)}$ = f(T_j); I_D = 2 A; V_{GS} =6V

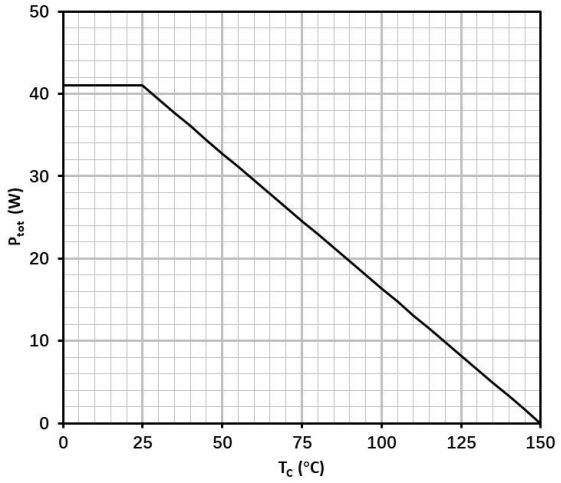
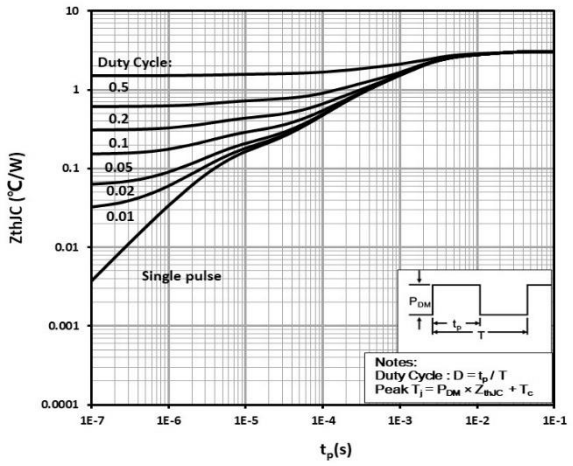
Figure 14 Power dissipation	Figure 15 Max.transient thermal impedance
	
P_{tot} = f(T_C)	Z_{thJC} = f(t_P, D)

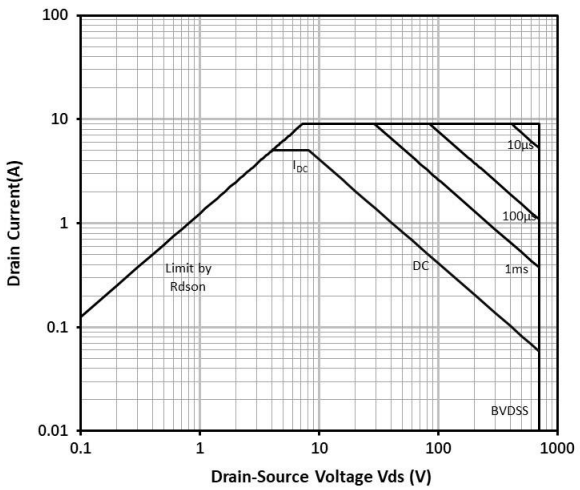
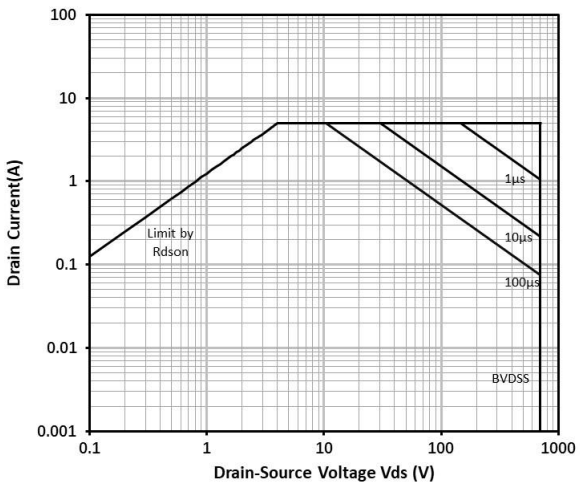
Figure 16 Safe operating area	Figure 17 Safe operating area
	
$I_D = f(V_{DS})$; $T_C = 25$ °C	$I_D = f(V_{DS})$; $T_C = 125$ °C

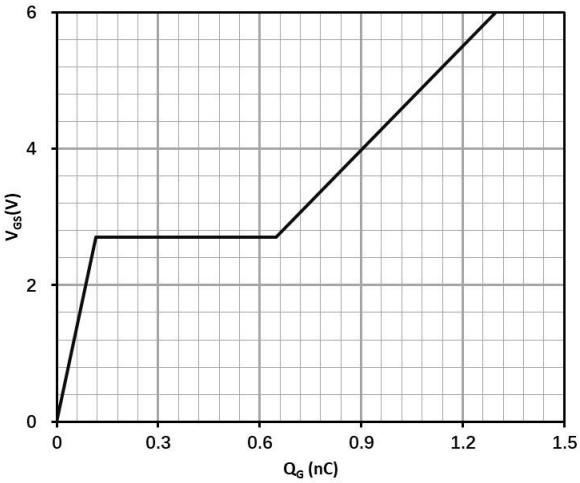
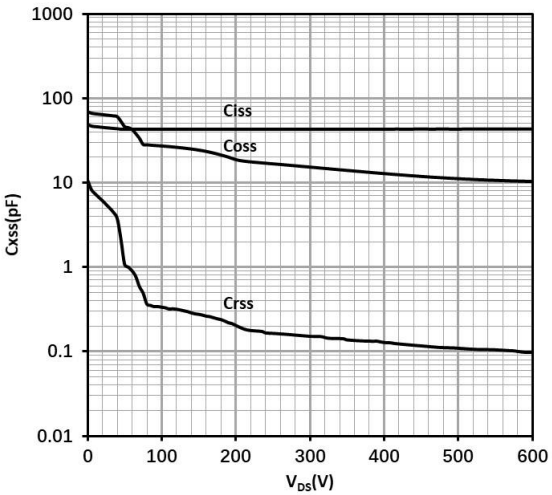
Figure 18 Typ. gate charge	Figure 19 Typ. capacitances
	
$V_{GS} = f(Q_G)$; $V_{DCLINK} = 400$ V; $I_D = 2$ A	$C_{XSS} = f(V_{DS})$;Freq. = 100 kHz

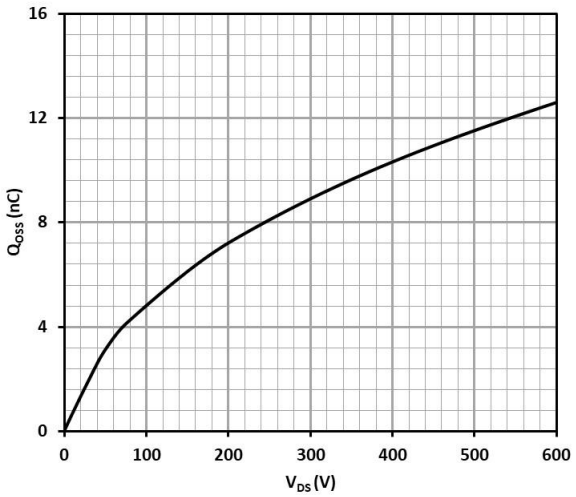
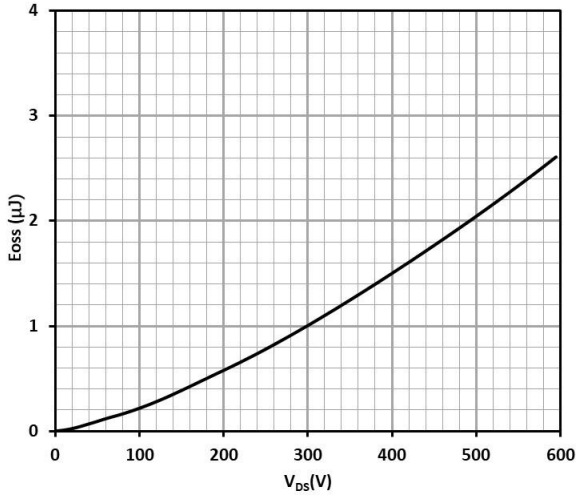
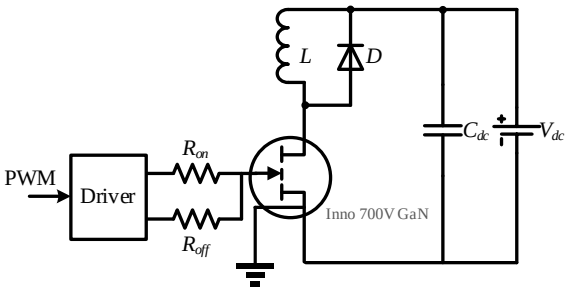
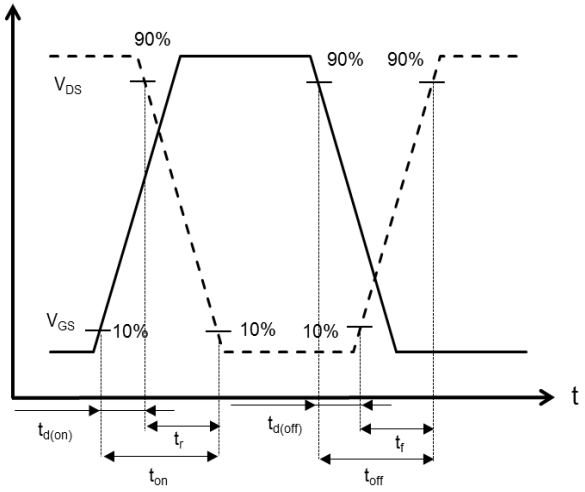
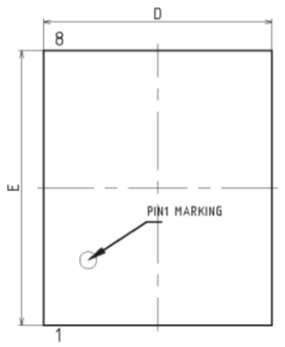
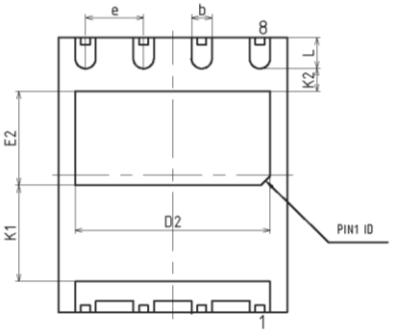
Figure 20 Typ. output charge	Figure 21 Typ. C_{OSS} stored Energy
	
Q_{OSS} = f(V_{DS});Freq. = 100 kHz	E_{OSS} = f(V_{DS});Freq. = 100 kHz

Figure 22 Typ.Switching times with inductive load	Figure 23 Typ.Switching times waveform
	
V_{DS} = 400 V, I_D = 4 A, L = 318 µH, V_{GS} = 6 V, R_{on} = 10 Ω, R_{off} = 2 Ω	

10. Package outlines

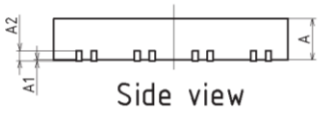


Top view

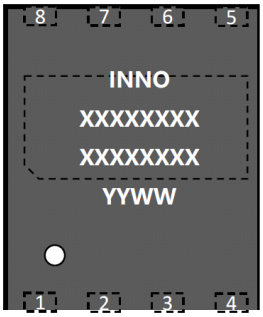


Bottom view

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.203REF	
b	0.40	0.45	0.50
D	4.90	5.00	5.10
D2	4.16	4.26	4.36
e		1.27	
E	5.90	6.00	6.10
E2	1.95	2.05	2.15
L	0.575	0.675	0.775
K1		2.10REF	
K2		0.50REF	



Side view



Row	Description	Example
Row1	Company name	INNO
Row2	Product code (In short)	XXXXXXXX
Row3	ASSY lot No.	XXXXXXXX
Row4	Date code	YYWW

Notes:

(1) Dimension and tolerance conform to ASME Y14.5-2009.

(2) All dimension are in millimeters.

(3) Lead coplanarity shall be 0.1 millimeters max.

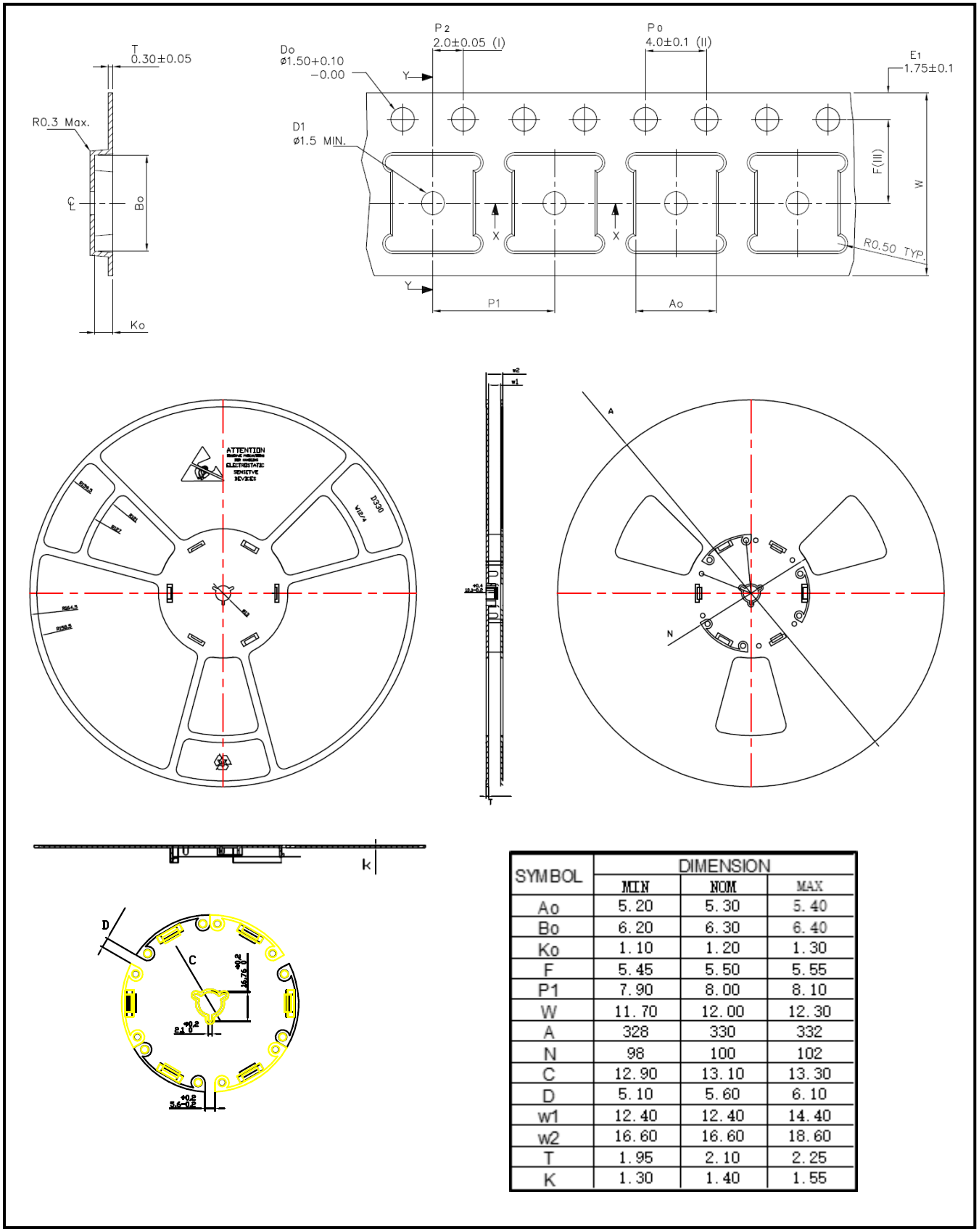
(4) Complies with JEDEC MO-229.

(5) Drawing is not to scale.

(6) Dimensions do not include mold protrusion.

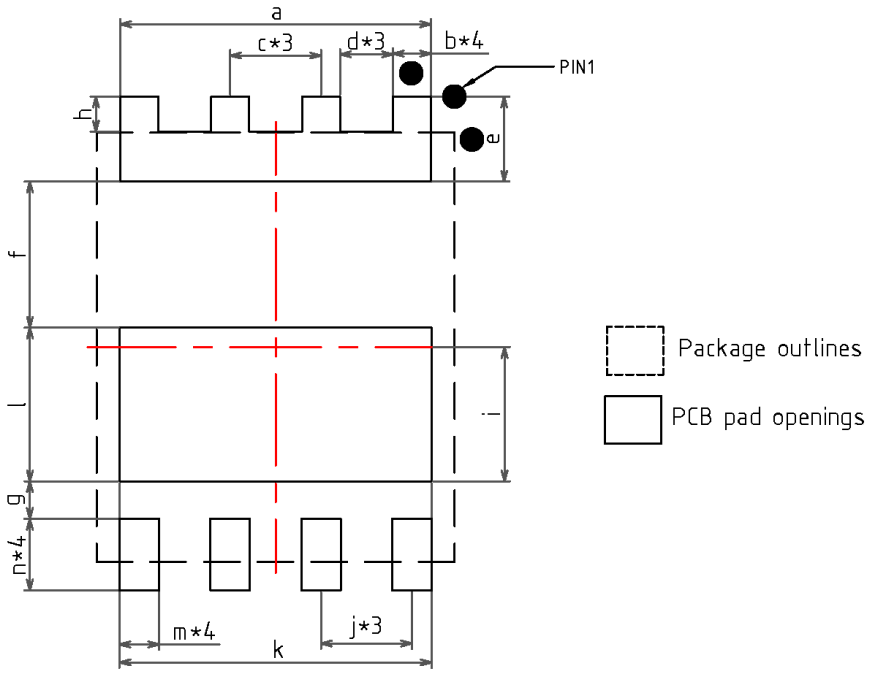
(7) Package outline exclusive of metal burr dimensions.

11. Reel information



SYMBOL	DIMENSION		
	MIN	NOM	MAX
Ao	5.20	5.30	5.40
Bo	6.20	6.30	6.40
Ko	1.10	1.20	1.30
F	5.45	5.50	5.55
P1	7.90	8.00	8.10
W	11.70	12.00	12.30
A	328	330	332
N	98	100	102
C	12.90	13.10	13.30
D	5.10	5.60	6.10
w1	12.40	12.40	14.40
w2	16.60	16.60	18.60
T	1.95	2.10	2.25
K	1.30	1.40	1.55

12. Recommended PCB footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	4.340	h	0.490
b	0.530	i	1.875
c	1.270	j	1.270
d	0.740	k	4.360
e	1.190	l	2.150
f	2.040	m	0.550
g	0.525	n	1.000

Notes:
(1)All dimension are in millimeters.
(2)Drawing is not to scale.

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-04-21	1.0 version release

Important Notice

The information provided in this document is intended as a guide only and shall not in any event be regarded as a guarantee of conditions, characteristics or performance. Innoscience does not assume any liability arising out of the application or use of any product described herein, including but not limited to any personal injury, death, or property or environmental damage. No licenses, patent rights, or any other intellectual property rights is granted or conveyed. Innoscience reserves the right to modify without notice.